UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,435	12/23/1999	MICHAEL J. MCTAGUE	INTL-0296-US	7390

7590 10/17/2005

TIMOTHY N TROP
TROP PRUNER HU & MILES PC
8554 KATY FREEWAY
SUITE 100
HOUSTON, TX 77024

EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/471,435
Filing Date: December 23, 1999
Appellant(s): MCTAGUE ET AL.

TIMOTHY N. TROP
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 07/21/2005 appealing from the Office action mailed on 03/17/2005.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the Appeal Brief filed on 07/21/2005.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner, which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,389,063 B1	KANEKAWA ET AL.	05-2002
6,603,807 B1	YUKUTAKE ET AL.	08-2003
6,359,926 B1	ISAKSSON ET AL.	03-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 3-7, 9-15, 17-28 and 30 are rejected under 35 U.S.C. 103(a). The rejection is set forth in the prior Office action, mailed on 03/17/2005 and repeated below, with additional details added, for the convenience of the board. Before answering appellant's arguments, it is worthwhile to review the problem being addressed by appellants' invention.

The problem being addressed, in general, is an asymmetric digital subscriber loop modem comprising two integrated circuits. Appellants claim that one of the integrated circuits contains an analog-to-digital converter producing at a relatively higher data rate, a device coupled to the analog-to-digital converter for reducing the higher data rate data from the analog-to-digital converter to a lower data rate data, and a multiplexer for multiplexing the lower data rate data and control information and transmit

the data and control information externally of the integrated circuit. Appellants further claims the other integrated circuit includes a de-multiplexer to de-multiplex the lower data rate data and the control information.

The Examiner's position is that the prior art references cited, applied to the same field of endeavor, teach all the limitations of the claimed subject matter including the motivation for combining them as explained in the prior Office action and repeated below with additional details.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-7, 9-10, 14-15, 17, 20-23, 25-26, 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanekawa et al. U.S. 6,389,063 B1 in view of Yukutake et al. U.S. 6,603,807 B1.

Regarding claim 1, Kanekawa et al. invention is directed to an insulating coupler, or insulating amplifier, or an isolator utilized for electrically separating and insulating between circuits, and a modem utilizing the isolator. In particular, Kanekawa et al. invention utilizes a highly dielectric capacitor that does not break

down the device (e.g. a modem in figure 20) and prevents a dangerous voltage from passing the secondary side even if a high voltage is applied.

In column 12 line 1 through column 13 line 35, figure 20 shows a constitution of a modem including a DC blocking switch 204, an analog front end (AFE) 100, and a host 203. The host 203 executes modulation of a sending signal, demodulation of a receiving signal, filtering, and other necessary processes, wherein the host 203 is further realized by a DSP (digital signal processor).

Figure 23 shows a constitution of AFE 100, wherein a clock signal CLK inputted from the host side is transmitted the subscriber line side via an isolating capacitor 2-0 of an isolator 50-0. Control circuits 101 and 102 exchange necessary control information via isolators 2-1 and 2-2 of isolators 50-1 and 50-2.

Kanekawa et al. does not expressly show the AFE 100 includes the first integrated circuits as set forth in the application claim.

As explained in the Response of Arguments in the prior Office action, in column 7 lines 35-40, Kanekawa et al. teaches in figure 6 shows the isolating capacitor 2 formed on a monolithic integrated circuit (IC) [Emphasis added]. Yukutake et al. further teaches a multi-channel capacitive isolator which is formed into a monolithic isolator chip as shown in figure 21e; see column 25, lines 25-45, see also figure 21e. Also in Yukutake et al. invention, in column 8, lines 45-64, application for using a multi-channel monolithic isolator is shown in figure 2, wherein the multi-channel monolithic isolator occupies the isolator 602

to insulate and separate the circuit areas 601 603. The circuit areas 601 603 form an analog I/O circuit area 601, and a digital I/O side circuit area 603. In light of Yukutake et al. foregoing teachings, one of ordinary skill in the art at the time of the invention would have been motivated that isolating capacitors 2-0 2-1 and 2-2 of an isolators 50-0 50-1 and 50-2 as taught by Kanekawa et al. can be formed on the same monolithic IC, as taught in Yukutake et al. invention. As result of the aforementioned teachings, there is no *hindsight rejection reasoning* as argued by Appellants, on the contrary, Kanekawa et al. and Yukutake et al. explicitly teach the capacitive isolator can be formed on a monolithic IC. As stated in previous Office action, the motivation for modifying Kanekawa et al. to include a portion of Yukutake et al. teachings is that Kanekawa et al. and Yukutake et al. teachings are in the same field of endeavor and disclose utilization of isolating capacitors formed on a monolithic IC in modem application. Both teachings teach the isolators being employed on an analog front end of a modem to electrically separate and insulate the analog I/O side and digital I/O side as discussed in Yukutake et al. teachings, the analog I/O side and digital I/O side corresponding to the subscriber line side and the host side as taught in Kanekawa et al. invention.

Referring back to figure 23 of Kanekawa et al. invention, the first region connecting to the subscriber line side includes an analog-to-digital converter (ADC) 105 producing data at a relatively higher data rate due to oversampling, a multiplexer 111 for multiplexing the data rate and coded control information from

the control circuit 101. A second region, connecting to the host side, includes a demultiplexer 112 for demultiplexing the data rate and control information, and a low pass filter and decimator 106 for reducing the data rate.

Kanekawa et al. does not show the low pass and decimator 106 coupled to ADC 105 for reducing higher data rate from ADC 105 as claimed in the pending application.

Although Kanekawa teaches a low pass filter and decimator 106 for reducing the data rate data, however, the arrangement of the low pass filter and decimator 106 is not between ADC 105 and MUX 111 as claimed in the pending application, see also figure 23. For that reason, the Examiner relies on a secondary reference, Yukutabe et al. US 6,603,807 B1, to show that a decimator can be arranged on the same side and located between ADC 105 and MUX 111. The location of the decimator as taught by Yukutabe et al. would be more advantageous than Kanekawa teachings since lower digital data rate is associated with much lower bit error rate as common knowledge of a person of ordinary skill in the art at the time of the invention.

Yukutake et al. discloses a very similar AFE arrangement (see figure 2) in another US patent wherein a decimator 515 coupled to ADC 514 for reducing higher data rate from ADC 514 to transmit the lower data rate data across isolators. In column 7, lines 40-60, because the output of the decimator (DCM) 515 is 16 bit wide, Yukutake et al. teaches that the data speed slows down so that the DCM 515 serially converts the 16-bit wide output to 2 Mega samples per

second and transmits it to the in-DSP 517 via the ADCR 516 of the I/O side circuit together with the timing signal via the isolator 502.

Kanekawa et al. invention and Yukutake et al. invention both teach utilization high capacitive insulator. Kanekawa et al. invention and Yukutake et al. explicitly teach the capacitive isolator can be formed on a monolithic integrated circuit (IC). Yukutake et al. goes further by realizing a multi-chip module having a primary side circuit IC, a secondary side circuit IC, and an IC circuit. Since lower digital data rate is associated with much lower bit error rate as common knowledge of a person of ordinary skill in the art, therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention that low-pass filter and decimator 106 as taught in figure 23 of Yukutabe et al. invention can be modified to be located between ADC 105 and MUX 111 to reduce the data rate data before transmitting lower data rate to the host side. The object of Kanekawa invention is to provide an information transmission system via an isolating capacitor having little error effect due to electrical noise. As common knowledge of a person of ordinary skill in the art at the time of the invention, high-speed digital link is susceptible to higher bit error rate due to timing jitters, which cause incorrect sampling of bit intervals. In view of the foregoing discussion, one of ordinary skill in the art would have been motivated to reduce the high data rate data by utilizing a decimator taught in Yukutabe et al. invention before transmitting across the isolator. Further evidence in figure 1 of Yukutabe et al. invention shows that lower-speed digital data is transmitted across isolator 501 to

interpolation filter 523, which interpolates (increase) the digital data to higher data rate data before converting it back to analog signals.

Furthermore, Kanekawa et al. teaches in column 13, line 1 to 5 that in the ***over-sampling system***, the digital data need to be reduced to a low sampling frequency before outputting to the host. Referring back to figure 23 of Kanekawa et al. invention, MUX 111 is for combining and sending serial data and control information across isolator. Because MUX 111 can operate at high data rate, slowing down the data rate before multiplexing step would have no effect on the operation of MUX 111.

As result of the modification, with low pass filter and decimator 106 coupled between ADC 105 and MUX 111, MUX 111 multiplexes lower data rate data and coded control information and transmit lower data rate data and coded control information externally of the first region on the subscriber line side, corresponding to the claimed first integrated circuit, to the region on the host side isolated from the subscriber line side via an isolating capacitor 2-1 of an isolator 50-1. The region on the host side, corresponding to the claimed second integrated circuit, includes a de-multiplexer DE-MUX 112 for de-multiplexing lower data rate data and coded control information as claimed in the pending application.

Regarding claims 3 and 25, with the modification as recited in claim 1, low pass filter and decimator 106 coupled between ADC 105 and MUX 111 in the region on subscriber line side includes a decimation filter as claimed.

Regarding claim 4, with the modification as recited in claim 1, referring to figure 23 above, the first region, corresponding the claimed first integrated circuit as discussed in claim 1, includes an analog pre-filter 104, corresponding to the claimed analog filter, wherein the analog pre-filter 104 is coupled to ADC 105 in turn coupled to low pass filter and decimator 106 in turn coupled to MUX 111.

Regarding claim 5, referring to figure 23 again, the region on the subscriber line side includes a DE-MUX 113 (de-multiplexer) coupled to a digital-to-analog converter (DAC) 109. Kanekawa et al. does not show a device that increases the data rate of data received by a de-multiplexer as claimed. Nevertheless, using analogous reasoning and motivation as for claim 1 when modifying Kanekawa et al. AFE 100 to couple low pass filter and decimator 106 between ADC 105 and MUX 111, a low pass filter and interpolator 110 in the region on the host side can be modified to locate in the region on the subscriber line side between DE-MUX 113 and a DAC 109 for interpolating a digital signal transmitted from the host side to a signal at the over-sampling frequency.

Regarding claims 6 and 26, as recited in claim 5, a low pass filter and interpolator 110 includes an interpolation filter.

Regarding claim 7, referring to figure 23, the region on the subscriber line side further includes a sending amplifier 107, and a receiving amplifier 103, wherein both sending amplifier 107, and receiving amplifier 103 are representative of both a receiver section and a transmitter section as appreciated by one of ordinary skill in the art.

Regarding claim 9, as recited in claim 1, the host 203 connected to the analog front end 100 executes modulation of a sending signal, demodulation of a receiving signal, filtering, and other necessary processes, wherein the host 203 is realized by a DSP (digital signal processor). As appreciated by one of ordinary skill in the art that, discrete multi-tone modulation (DMT) is known to be implemented in digital subscriber line (DSL) modem such as the modem illustrated in figure 20. Even though Kanekawa et al. does not expressly teach DMT implemented in the modem of figure 20, one of ordinary skill in the art would have been motivated to implement discrete multi-tone modulation in Kanekawa et al. modem because Kanekawa et al. expresses that the host 203 can be realized by a DSP which is known to implement DMT in the modem.

Regarding claim 10, as recited in claim 1, the host 203 connected to the analog front end 100 executes modulation of a sending signal, demodulation of a receiving signal, filtering, and other necessary processes, wherein the host 203 is realized by a DSP (digital signal processor).

Regarding claim 14, claim 14 is rejected on the same ground as for claim 1 because of similar scope. Referring to figure 23, on the subscriber line side, a receiving amplifier 103 receives an analog data. ADC 105 converts the analog data into digital format.

Kanekawa et al. does not show the step of decreasing the data rate of said data on the subscriber line side as claimed. Kanekawa et al., however, discloses a low pass filter and decimator 106 for reducing the data rate on the host side. Using analogous reasoning and motivation as for claim 1 to modify Kanekawa et al. AFE 100 to couple low pass filter and decimator 106 between ADC 105 and MUX 111 on the subscriber line side.

With the modification, low pass filter and decimator 106 reduces the data rate data from ADC 105. As appreciated by one of ordinary skill in the art, MUX 111 performs both serialization of data and multiplexing serialized data with coded control information. MUX 111 transmits serialized data with coded control information to the region on host side isolated from the subscriber line side via an isolating capacitor 2-1 of an isolator 50-1.

In the region on host side, a DE-MUX 112 de-multiplexes serialized data with coded control information. As recited in claim 1, the region on the host side including the host 203 is equivalent to the second integrated circuit for the reason as stated in claim 1.

Regarding claim 15, with the modification as recited in claim 1, low pass filter and decimator 106 coupled between ADC 105 and MUX 111 on the subscriber line side performs decimating the digital data.

Regarding claim 17, similar to the reasoning for MUX 111 as recited in claim 14, as appreciated by one of ordinary skill in the art that the demultiplexing process of DE-MUX 112 demultiplexes data into individual data streams. In view of that, the process corresponds to deserializing digital data as claimed.

Regarding claim 20, referring back to figure 23, Kanekawa et al. shows a low pass filter and interpolator 110 for increasing the data rate of the data the region on the host side, corresponding to the second integrated circuit as explained in claim 1. Using analogous reasoning and motivation as for claim 5, it would have been obvious for one of ordinary skill in the art that the low pass filter and interpolator 110 can be modified to couple between DE-MUX 113 and DAC 109 for increasing the data rate of the data as claimed. The region of the subscriber line side receives digital data transmitted from the region on host side.

Regarding claim 21, as recited in claim 20, the low pass filter and interpolator 110 includes an interpolator for interpolating said data.

Regarding claim 22, DAC 109 converts digital data back to an analog format signal.

Regarding claim 23, using analogous reasoning and motivation as for claim 1 due to similar scope, referring back to figure 23, the region on the subscriber line side, equivalent to the claimed first integrated circuit, includes ADC 105, MUX 111 corresponding to the claimed serializer. The low pass filter and decimator 106 for reducing the data rate data, corresponding to the claimed device, is on the region on the host side. However, with the modification and motivation as stated in claim 1, low pass filter and decimator 106 can be modified to couple between ADC 105 and MUX 111 on the region of the subscriber line side.

In view of that, MUX 111 multiplexes lower data rate data and coded control information and transmit lower data rate data and coded control information externally of the first region on the subscriber line side, corresponding to the claimed first integrated circuit, to the region on the host side isolated from the subscriber line side via an isolating capacitor 2-1 of an isolator 50-1. The region on the host side, corresponding to the claimed second integrated circuit, includes a de-multiplexer corresponding to the claimed de-serializer, wherein DEMUX 112 for de-multiplexing lower data rate data and coded control information before transmitting to the host 203.

Regarding claim 28, Kanekawa et al. does not expressly disclose the modem in figure 20 is splitterless. However, the modem in figure 20 suggests a splitterless modem as appreciated by one of ordinary skill in the art.

Regarding claim 30, referring to figure 23 again, lower data rate data is transmitted to the region on host side through low pass filter and decimator 106, and to the region on subscriber line side through low pass filter and interpolator 110. In view of that, lower data rate data is transmitted in two directions as claimed in the pending application.

Claims 11, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanekawa et al. U.S. 6,389,063 B1 and Yukutake et al. U.S. 6,603,807 B1 as applied to claim 9 and further in view of Isaksson et al. U.S. Patent 6,359,926 B1.

Regarding claim 11, since the host 203 executes modulation of a sending signal, demodulation of a receiving signal, filtering, and other necessary processes, the host 203 includes a line decoder as appreciated by one of ordinary skill in the art. Furthermore, DMT system is well known in the art of DSL modem, and is discussed in Isaksson et al. invention. Figure 4 illustrates a DMT transceiver including an analog front end and a digital receiver unit and a digital transmitter unit. Since Kanekawa et al. modem can be modified to implement DMT which always utilizes a Fourier transformer and an inverse Fourier transformer, it would have been obvious for one of ordinary skill

in the art at the time the invention was made that the host 203 can be modified to include a Fourier transformer as that shown in figure 4 of Isaksson et al. invention.

Regarding claim 18, said claim is rejected using analogous argument as for claim 11. The fast Fourier transformer included in the host 203 effectively increases the data rate due to the Fourier transform process as known in the art of DSL modems.

Regarding claim 19, as recited in claim 18, said claim is rejected using analogous argument as for claim 11. In claim 11, the host 203 is modified to implement DMT, resulting utilization of a fast Fourier transformer.

Claims 12-13, 24, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanekawa et al. U.S. 6,389,063 B1 and Yukutake et al. U.S. 6,603,807 B1 as applied to claim 1 and further in view of Isaksson et al. U.S. Patent 6,359,926 B1.

Regarding claim 12, claim 1 rejection argument addresses all the limitations of claim 12, except the limitation encompassing a second integrated circuit as set forth in claim 12. As recited in claim 1, the host 203 executes modulation of a sending signal, demodulation of a receiving signal, filtering, and other necessary processes, the host 203 includes a line encoder as appreciated by one of ordinary skill in the art. Furthermore, using analogous reasoning and motivation as for claim 11, DMT system is well known in the art of DSL modem, and is discussed in Isaksson et al. invention.

Since Kanekawa et al. modem can be modified to implement DMT, it would have been obvious for one of ordinary skill in the art at the time the invention was made that the host 203 can be modified to further include a scaling and inverse fast Fourier transformer (IFFT) as shown in figure 4 of Isaksson et al. invention.

Regarding claims 13 and 27, as recited in claim 12, the host 203 also includes a scaling and inverse fast Fourier transformer (IFFT) similar to that shown in figure 4 of Isaksson et al. invention.

Regarding claim 24, claims 13 and 24 are very similar in scope. Claim 24 is rejected on the same ground as claim 13. The modulating circuit for decreasing the data rate of digital data in claim 24 corresponds to an inverse fast Fourier Transformer, which has been rejected as stated in claim 13. The serializer on the second integrated circuit in claim 24 corresponds to a serializer in claim 12 on which claim 13 depends.

However, claim 13 does not address the first integrated circuit including a de-serializer as set forth in claim 24. The de-serializer as set forth in claim 24 has been addressed in the rejection of claim 5 wherein DE-MUX 113 performs equivalent function of a de-serializer.

Furthermore, as recited in claim 5, referring to figure 23 again, the region on the subscriber line side includes a DE-MUX 113 (de-multiplexer) coupled to a digital-to-analog converter (DAC) 109. Kanekawa et al. does not show a low pass

filter and interpolator 110 in the region on the subscriber line side, corresponding to the claimed device that increases the data rate of data received by a de-multiplexer as claimed. Nevertheless, using analogous reasoning and motivation as for claim 1 when modifying Kanekawa et al. AFE 100 to couple low pass filter and decimator 106 between ADC 105 and MUX 111, a low pass filter and interpolator 110 in the region on the host side can be modified to locate in the region on the subscriber line side between DE-MUX 113 and a DAC 109 for interpolating a digital signal transmitted from the host side to a signal at the oversampling frequency.

(10) Response to Argument

Appellant argues, on page 12, of the Appeal Brief that "Neither of the cited references teach a multiplexer to multiplex said lower data rate data and control information and transmit the data and control information externally of said integrated circuit. With respect to the reference to Yukutake, it appears that the Examiner is taking the position that somehow the use of the isolators 501 and 502, in Figure 1, teach the use of separate circuits".

Examiner's position is to address the issue "the Examiner is taking the position that somehow the use of the isolators 501 and 502, in Figure 1, teach the use of separate circuits". As recited in the Final rejection and the Advisory action, expressly

taught in figure 23 of Kanekawa et al. invention, isolating capacitors 2-0 2-1 ... of an isolators 50-0 50-1 50-2 ... are employed to isolate the region on the host side from the subscriber line side; see column 12 line 25 through column 13 line 35, see also figures 21 22 23.

Similarly, in column 8, lines 45-67, Yukutake et al. teaches the layout as shown in figure 2, the circuit areas 601 602 603 are enclosed by trenches so as to form an analog I/O side circuit area 601, an isolator area 602, and a digital I/O side circuit area 603. By enclosing each circuit block in the circuit areas 601 to 603, the circuits are insulated and separated from each other and the devices are separated [Emphasis added]. Due to the layout as shown in figure 2 of Yukutake et al. invention, the circuit areas 601 602 603 are separate areas and insulated from each other. And as recited above, because the isolator area 602 can be implemented on a monolithic integrated circuit, one of ordinary skill in the art of integrated circuit technology would have been motivated to implement the circuit areas 601 and 603 on separate integrated circuits. The motivation is shown in column 25 lines 45-65 of Yukutake et al. invention that figure 21f is a plane view of a multi-chip module (hereinafter called as MCM) having a monolithic isolator. Numeral 6 is a **multi-channel monolithic isolator chip**, numeral **7 is a primary side peripheral circuit integrated circuit (IC)**, and numeral **8 is a secondary side peripheral circuit integrated circuit (IC)**. In column 26, lines 50-67, Yukutake et al. further teaches that the analog front end, e.g. as shown in figures 1 and 2, comprises a primary and secondary side circuits provided on the semiconductor substrate and insulated from each other by a capacitive insulating means positioned on

the semiconductor substrate for transferring signals between the primary side circuit and secondary side circuit.

In light of Yukutake et al. foregoing teachings and motivation as shown figure 21f, contrary to Appellants' arguments recited above, one of ordinary skill in the art would have recognized that Kanekawa et al. teachings in figure 23 can be modified in such a way that the region on the host side, the region on the subscriber line side, and isolating capacitors 2-0 2-1 ... of an isolators 50-0 50-1 50-2 can be implemented on separate integrated circuits, e.g. a primary side peripheral circuit IC, a secondary side peripheral circuit IC, and a multi-channel monolithic isolator chip as taught in Yukutake et al. invention.

Examiner's position to "Neither of the cited references teach a multiplexer to multiplex said lower data rate data and control information and transmit the data and control information externally of said integrated circuit".

Referring to Kanekawa et al. invention, in rejecting claims 1, 3-7, 9-10, 14-15, 17, 20-23, 25-26, 28 and 30, the Examiner relies on the main reference, Kanekawa et al. U.S. Patent 6,389,063 B1 to teach most of the claimed features [Emphasis added]. As recited in the Final rejection and repeating again, figure 23 shows a constitution of AFE 100, wherein a clock signal CLK inputted from the host side is transmitted the subscriber line side via an isolating capacitor 2-0 of an isolator 50-0. Control circuits 101 and 102 exchange necessary control information via isolators 2-1 and 2-2 of isolators 50-1 and 50-2. The first region connecting to the subscriber line side includes an analog-to-digital converter (ADC) 105 producing data at a relatively higher data rate

data due to over-sampling, a multiplexer 111 for multiplexing the data rate data and control information from the control circuit 101.

Kanekawa et al. invention differs from the claimed invention in that the higher data rate data is not reduced before multiplexing with control information, and transmitting data and control information externally of the integrated circuit.

As recited in the Final rejection, although Kanekawa teaches a low pass filter and decimator 106 for reducing the data rate data, however, the arrangement of the low pass filter and decimator 106 is not between ADC 105 and MUX 111 as claimed in the pending application, see also figure 23. For that reason, the Examiner relies on a secondary reference, Yukutabe et al. US 6,603,807 B1, to show that a decimator can be arranged on the same side and located between ADC 105 and MUX 111. The location of the decimator as taught by Yukutabe et al. would be more advantageous than Kanekawa teachings since lower digital data rate is associated with much lower bit error rate as common knowledge of a person of ordinary skill in the art.

As taught in column 7, lines 40-60, and referring to figure 1, Yukutake et al. teaches that the ADC 514 operates at 2 Msps (mega samples per second) and transmits this AD conversion output to the DCM 515. The output of the DCM 515 is 16 bit/w. However, the speed is slowing to 32 ksps (kilo samples per second), so that the DCM515 serially converts the digital stream and transmits it to the in-DSP 517 via the ADCR 516 of the I/O side circuit together with the timing signal via the isolator 502.

Kanekawa et al. teaches other claimed limitations, but lacks the step of reducing the higher data rate data by a decimator *before multiplexing* with control information, and transmitting data and control information externally of the integrated circuit.

Kanekawa et al. invention and Yukutake et al. invention are similar in that both teach utilization high capacitive insulator. Kanekawa et al. invention and Yukutake et al. explicitly teach the capacitive isolator can be formed on a monolithic integrated circuit (IC). Yukutake et al. teachings further suggest that the isolator can be realized as a multi-chip module having a primary side circuit integrated circuit (IC), a secondary side circuit integrated circuit (IC), and an IC circuit. Since lower digital data rate is associated with much lower bit error rate as common knowledge of a person of ordinary skill in the art, therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention that low-pass filter and decimator 106 as taught in figure 23 of Yukutabe et al. invention can be modified to be located between ADC 105 and MUX 111 to reduce the data rate data before transmitting lower data rate to the host side since Yukutabe et al. suggests in column 7, lines 40-60 to slow down the data rate such that serial data is transmitted together with the timing signal via the isolator 502. First, the object of Kanekawa invention is to provide an information transmission system via an isolating capacitor having little error effect due to electrical noise. As common knowledge of a person of ordinary skill in the art at the time of the invention, high-speed digital link is susceptible to higher bit error rate due to timing jitters, which cause incorrect sampling of bit intervals. In view of the foregoing discussion, one of ordinary skill in the art would have been motivated to reduce the high data rate data by utilizing a decimator taught in

Yukutabe et al. invention before transmitting across the isolator. Further evidence in figure 1 of Yukutabe et al. invention shows that lower-speed digital data is transmitted across isolator 501 to interpolation filter 523, which interpolates (increase) the digital data to higher data rate data before converting it to analog signals.

Appellant argues, on pages 12-13, of the Appeal Brief that "But, even if one were to accept this relatively unusual proposition, it still fails to meet the claimed invention. This is because there is a fundamental difference in the way the circuits in Yukutake and the claimed invention work. In the cited reference, the so-called decimeter "515" is apparently asserted to reduce the higher data rate. But, even if that is so, it also serializes the data. See column 7, lines 49-50. Thus, it is assumed that the device 515 is read to be the device for reducing the higher data rate in claim 1, as well as the multiplexer to multiplex said lower data rate data and control information. However, the claim further calls for a second integrated circuit, which, apparently, the Examiner contends to be the stuff downstream of the isolator 502 by virtual of isolator 502 allegedly functioning as if there were a separate integrated circuit. The problem is that the claim requires that the second integrated circuit include a demultiplexer to de-multiplex the lower data rate. In the cited reference, all of the data going through the ADCR 516 in-DSP 517, RDR 518, eX-DSP 536 and returning through the TDR 521, in-DSP 517 is still serial data. The serial conversion is done in the DACR 522. See column 7, line 65. In other words, there does not appear to be any type of de-multiplexing or de-serialization on the other side of the isolators 502 and 501 from the DCM 515 and WT

523. Thus, there is no isolation between serialized and un-serialized data. All the serialized data is handled on the same side of the isolators. In order for the analogy the Examiner is asserting to work, he would have to show that on the other side of the isolator 501, the data is de-serialized, for example, on ADCR 516. However, there is no indication that this is done in the cited reference

Kanekawa cannot help with this deficiency since Kanekawa does not teach reducing the data rate. See the office action at page 7, lines 9-12. That is why the Examiner is relying on Yukutake. The premise of the Examiner's position seems to be that because two references teach using a single integrated circuit with isolation devices in between regions thereof, that somehow the combination of these two references teaches using separate integrated circuits. An assertion of equivalency is not sufficient to meet the claimed invention. It does not matter whether the two circuits are functional equivalents. What matters is whether or not anything teaches what is claimed.

As explained in the Background of the present application at page 2, line 15, existing modems generally are implemented using two or more integrated circuits. One set of integrated circuits provides most of the digital signal processing and the other provides the analog to digital and digital to analog conversion. Generally, the two integrated circuits are separated after A to D conversion on the receiver side and before D to A conversion on the transmitter side. This means that data is transmitted between the two chips at relatively high data rates. This high data rate transmission results in more buffering on each chip and more pins are needed to connect the chips. This increases the cost of each chip. In addition, the high data rate results in higher system

cost due to the impact of higher frequency operation and electromagnetic interference shielding. Thus, the problem that was sought to be overcome is the one of using two separate integrated circuits, but transmitting the data between them at high data rates. Nothing in any of the cited references suggest slowing down the data rate before transferring the data between two spaced integrated circuits. This failure of teaching makes the rejection insufficient to make out a prima facie rejection. Nothing has addressed the problem solved by the claimed invention. Neither of the two cited references are even faced with the same problem. Both of the two references use a single integrated circuit as plainly depicted in their figures. The fact that they, according to the Examiner, contemplated having isolating capacitors that are separate integrated circuits is noted, but, there is no transmission between two separate integrated circuits in any of the cited references".

Examiner's position is that referring back to claim 1 of the instant application, claim 1 calls for a multiplexer to multiplex the lower data rate data and control information and transmit the data and control information externally of the integrated circuit. In view of the claimed invention, the lower data rate data is a serial data stream and the multiplexer multiplexes the serial data stream with control information. The claim further calls for a second integrated circuit, said second integrated circuit including a de-multiplexer to *de-multiplex said lower data rate data and said control information*. Hence, the demultiplexer separates the lower data rate data and the control information.

Referring to Kanekawa et al. invention, as recited above, figure 23 shows a constitution of AFE 100, wherein a clock signal CLK inputted from the host side is transmitted the subscriber line side via an isolating capacitor 2-0 of an isolator 50-0. Control circuits 101 and 102 exchange necessary control information via isolators 2-1 and 2-2 of isolators 50-1 and 50-2. The first region connecting to the subscriber line side includes an analog-to-digital converter (ADC) 105 producing data at a relatively higher data rate data due to over-sampling, a multiplexer 111 for multiplexing the data rate data and coded control information from the control circuit 101. The second region connecting to the host side includes a demultiplexer for de-multiplexing the lower data rate data and control information.

However, Kanekawa et al. invention differs from the claimed invention in that the higher data rate data is not reduced before multiplexing with control information, and transmitting data and control information externally of the integrated circuit.

As recited in the Final rejection, although Kanekawa teaches a low pass filter and decimator 106 for reducing the data rate data, however, the arrangement of the low pass filter and decimator 106 is not between ADC 105 and MUX 111 as claimed in the pending application, see also figure 23. For that reason, the Examiner relies on a secondary reference, Yukutabe et al. US 6,603,807 B1, to show that a decimator can be arranged on the same side and located between ADC 105 and MUX 111. The location of the decimator as taught by Yukutabe et al. would be more advantageous than Kanekawa teachings since lower digital data rate is associated with much lower bit error rate as common knowledge of a person of ordinary skill in the art.

First, as discussed in column 2, lines 25-35, the object of Kanekawa invention is to provide an information transmission system via an isolating capacitor having little error effect due to electrical noise.

As taught in column 7, lines 40-60, and referring to figure 1, Yukutake et al. teaches that the ADC 514 operates at 2 Msps (mega samples per second) and transmits this AD conversion output to the DCM 515. The output of the DCM 515 is 16 bit/w. However, the speed is slowing to 32 ksps (kilo samples per second), so that the DCM515 serially converts the digital stream and transmits it to the in-DSP 517 via the ADCR 516 of the I/O side circuit together with the timing signal via the isolator 502.

Kanekawa et al. teaches the other claimed limitations, but lacks the step of reducing the higher data rate data by a decimator *before multiplexing* with control information, and transmitting data and control information externally of the integrated circuit.

Kanekawa et al. invention and Yukutake et al. invention are similar in that both teach utilization high capacitive insulator. Kanekawa et al. invention and Yukutake et al. explicitly teach the capacitive isolator can be formed on a monolithic integrated circuit (IC). Yukutake et al. teachings suggest further that the isolator can be realized as a multi-chip module having a primary side circuit integrated circuit (IC), a secondary side circuit integrated circuit (IC), and an IC circuit. Since lower digital data rate is associated with much lower bit error rate as common knowledge of a person of ordinary skill in the art, therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention that low-pass filter and decimator 106 as taught in figure 23 of Yukutabe et

al. invention can be modified to be located between ADC 105 and MUX 111 to reduce the data rate data before transmitting lower data rate to the host side since Yukutabe et al. suggests in column 7, lines 40-60 to slow down the data rate such that serial data is transmitted together with the timing signal via the isolator 502. First, the object of Kanekawa invention is to provide an information transmission system via an isolating capacitor having little error effect due to electrical noise. As common knowledge of a person of ordinary skill in the art at the time of the invention, high-speed digital link is susceptible to higher bit error rate due to timing jitters, which cause incorrect sampling of bit intervals. In view of the foregoing discussion, one of ordinary skill in the art would have been motivated to reduce the high data rate data by utilizing a decimator taught in Yukutabe et al. invention before transmitting across the isolator. Further evidence in figure 1 of Yukutabe et al. invention shows that lower-speed digital data is transmitted across isolator 501 to interpolation filter 523, which interpolates (increase) the digital data to higher data rate data.

Furthermore, Kanekawa et al. teaches in column 13, line 1 to 5 that in the ***over-sampling system***, the digital data need to be reduced to a low sampling frequency before outputting to the host. Referring back to figure 23 of Kanekawa et al. invention, MUX 111 is for combining and sending serial data and control information across isolator. Because MUX 111 can operate at high data rate, slowing down the data rate data before multiplexing step would have no effect on the operation of MUX 111. The act of slowing down the data rate data before multiplexing step would satisfy the

suggestion of reducing the digital data rate in an over-sampling system according to Kanekawa et al. suggestion.

Examiner's position addresses "the claim further calls for a second integrated circuit, which, apparently, the Examiner contends to be the stuff downstream of the isolator 502 by virtual of isolator 502 allegedly functioning as if there were a separate integrated circuit. The problem is that the claim requires that the second integrated circuit include a demultiplexer to de-multiplex the lower data rate".

As recited above, in column 25 lines 45-65 of Yukutake et al. teachings, figure 21f is a plane view of a multi-chip module (hereinafter called as MCM) having a monolithic isolator. Numeral 6 is a **multi-channel monolithic isolator chip**, numeral **7 is a primary side peripheral circuit IC**, and numeral **8 is a secondary side peripheral circuit IC**. Further, in column 26, lines 50-67, Yukutake et al. teaches that the analog front end, e.g. as shown in figure 1, comprises a primary and secondary side circuits provided on the semiconductor substrate and insulated from each other by a capacitive insulating means positioned on the semiconductor substrate for transferring signals between the primary side circuit and secondary side circuit. In view of that, Yukutake et al. does suggest a second integrated circuit for receiving the data and timing signal transmitted from the primary side circuit.

Yukutake et al. does not expressly show a demultiplexer for de-multiplexing the lower data rate and the timing signal as claimed by Appellant. However, in column 8, lines 5-20, Yukutake et al. further teaches that the processing timings are timings for synchronizing the analog I/O side circuit and digital I/O side circuit. Therefore, a person

of average skill in the art would have expected the timing signal is de-multiplexed (extracted) from the lower data rate data and timing signal for synchronizing purposes. Furthermore, referring to figure 23 of Kanekawa et al. invention, which the Examiner relies on as the main reference for the rejection, the demultiplexer (DEMUX) 112 de-multiplexes the control information (or timing signal as taught in Yukutake et al. invention) from the data. In light of the aforementioned teachings, contrary to Appellant's argument, Kanekawa et al. teaches a demultiplexer for de-multiplexing the data rate data and control information in the second integrated circuit.

Appellant argues that "more poignantly, if one were to accept the Examiner's proposition that the Kanekawa reference could be effectively considered to be split in two by virtual of the circuit elements 50 and 2, along a vertical line in Figure 23, the Examiner has then presented a reference which constitutes the prior art whose problems the present invention sought to overcome. In other words, the reference shown in Figure 23 is not even as close to the present invention as what was already discussed in the Background. If one were to modify that reference with no teaching in the prior art, to make two separate circuits, all one would have would be exactly the circuit that had the very problems set forth in the Background. The Examiner points to another reference, which still does not use separate integrated circuits. Neither reference teaches a solution to the problems arising from data transfer between separate chips. Since Yakutake used a single integrated circuit, there is nothing in Yakutake that would suggest the solution to the problems faced when separate

integrated circuits are used. Whatever reason Yakutake had for decimating the data had nothing to do with the problems that arise when separate integrated circuits are provided. That is necessarily so because Yakutake did not have separate integrated circuits. Thus, if one were to modify Kanekawa as proposed by the Examiner, he would then face all of the deficiencies noted in the Background. It seems illogical to suggest that he would appreciate the solution to those problems in a reference that does not even use two separate circuits and, therefore, does not even solve the problems. This is merely hindsight reasoning. It is the suggestion that decimation could be used to overcome problems because a reference teaches decimation for some other purpose. There is no suggestion of using the decimation before transferring the data from one integrated circuit to another. Therefore, the fact that decimation is used before data is transferred across regions of the same integrated circuit simply does not teach a solution to the problems solved by the present invention and faced by Kanekawa. In short, there is no teaching in any of the references or their combination of a solution to the problem only recognized by the present Appellants. Therefore, the rejection should be reversed".

Examiner's position is that as recited above, in column 25 lines 45-65 of Yukutake et al. teachings, figure 21f is a plane view of a multi-chip module (hereinafter called as MCM) having a monolithic isolator. Numeral 6 is a **multi-channel monolithic isolator chip**, numeral **7 is a primary side peripheral circuit IC**, numeral **8 is a secondary side peripheral circuit IC**, and numeral 16 is a package. Further, in column 26, lines 50-67, Yukutake et al. teaches that the analog front end, e.g. as shown in

figure 1, comprises a primary and secondary side circuits provided on the semiconductor substrate and insulated from each other by a capacitive insulating means positioned on the semiconductor substrate for ***transferring signals between the primary side circuit and secondary side circuit***.

In view of that, ***Yukutake et al. does suggest separate integrated circuits*** for transmitting and receiving the data and timing signal from the primary side circuit to the secondary side circuit. As recited above, because the output of the decimator (DCM) 515 is 16 bit wide, Yukutake et al. teaches that the data speed slows down so that the DCM 515 ***serially*** converts the 16-bit wide output to 2 Mega samples per second and transmits it to the in-DSP 517 via the ADCR 516 of the I/O side circuit together with the timing signal via the isolator 502. The transmission of the timing is necessary to synchronize the operation timing to prevent the degradation of a signal due to crosstalk.

As also recited above, Kanekawa et al. teaches the other claimed limitations, but lacks the step of reducing the higher data rate data by a decimator *before multiplexing* with control information, and transmitting data and control information externally of the integrated circuit.

Kanekawa et al. invention and Yukutake et al. invention are similar in that both teach utilization high capacitive insulator. Kanekawa et al. invention and Yukutake et al. explicitly teach the capacitive isolator can be formed on a monolithic integrated circuit (IC). Yukutake et al. teachings suggest further that the isolator can be realized as a multi-chip module having a primary side circuit integrated circuit (IC), a secondary side circuit integrated circuit (IC), and an IC circuit. Therefore, it would have been obvious for

one of ordinary skill in the art at the time of the invention that low-pass filter and decimator 106 as taught in figure 23 of Yukutabe et al. invention can be modified to be located between ADC 105 and MUX 111 to reduce the data rate data before transmitting lower data rate to the host side. First, the object of Kanekawa invention is to provide an information transmission system via an isolating capacitor having little error effect due to electrical noise. As common knowledge of a person of ordinary skill in the art at the time of the invention, high-speed digital link is susceptible to higher bit error rate due to timing jitters, which cause incorrect sampling of bit intervals. In view of the foregoing discussion, one of ordinary skill in the art would have been motivated to reduce the high data rate data by utilizing a decimator taught in Yukutabe et al. invention before transmitting across the isolator. Further evidence in figure 1 of Yukutabe et al. invention shows that slower-speed digital data is transmitted across isolator 501 to interpolation filter 523, which interpolates (increase) the digital data to higher data rate data.

In view of the foregoing teachings, contrary to Appellant's arguments, prior art does teach all claim limitations as discussed above. Furthermore, MPEP section 2144 guides that:

> " ***The reason or motivation to modify the reference may often suggest what the inventor has done, but for a different purpose or to solve a different problem. It is not necessary that the prior art suggest the combination to achieve the same advantage or result discovered by Appellant***. ***In re Linter*, 458 F.2d 1013, 173 USPQ 560 (CCPA 1972) (discussed below)**; *In re Dillon*, 919 F.2d 688, 16 USPQ2d 1897 (Fed. Cir. 1990), *cert. denied*, 500 U.S. 904 (1991) (discussed below). Although *Ex parte Levengood*, 28 USPQ2d 1300, 1302 (Bd. Pat. App. & Inter. 1993) states that obviousness cannot be established by

combining references "without also providing evidence of the motivating force which would impel one skilled in the art to do what the patent Appellant has done" (emphasis added), reading the quotation in context it is clear that while there must be motivation to make the claimed invention, **there is no requirement that the prior art provide the same reason as the Appellant to make the claimed invention**.

In *In re Linter* the claimed invention was a laundry composition consisting essentially of a dispersant, cationic fabric softener, sugar, sequestering phosphate, and brightener in specified proportions. The claims were rejected over the combination of a primary reference, which taught all the claim limitations except for the presence of sugar, and secondary references which taught the addition of sugar as a filler or weighting agent in compositions containing cationic fabric softeners. Appellant argued that in the claimed invention, the sugar is responsible for the compatibility of the cationic softener with the other detergent components. The court sustained the rejection, stating "The fact that appellant uses sugar for a different purpose does not alter the conclusion that its use in a prior art composition would be [sic, would have been] *prima facie* obvious from the purpose disclosed in the references." 173 USPQ at 562.

In *In re Dillon*, Appellant claimed a composition comprising a hydrocarbon fuel and a sufficient amount of a tetra-orthoester of a specified formula to reduce the particulate emissions from the combustion of the fuel. The claims were rejected as obvious over a reference, which taught hydrocarbon fuel compositions containing tri-orthoesters for dewatering fuels, in combination with a reference teaching the equivalence of tri-orthoesters and tetra-orthoesters as water scavengers in hydraulic (nonhydrocarbon) fluids. The Board affirmed the rejection finding "there was a 'reasonable expectation' that the tri- and tetra-orthoester fuel compositions would have similar properties based on 'close structural and chemical similarity' between the tri- and tetra-orthoesters and the fact that both the prior art and Dillon use these compounds 'as fuel additives'." 919 F.2d at 692, 16 USPQ2d at 1900. The court held "it is not necessary in order to establish a *prima facie* case of obviousness . . . that there be a suggestion or expectation from *the prior art* that the claimed [invention] will have the same or a similar utility as *one newly discovered by Appellant*," and concluded that here a *prima facie* case was established because "[t]he art provided the motivation to make the claimed compositions in the expectation that they would have similar properties." 919 F.2d at 693, 16 USPQ2d at 1901 (emphasis in original).

".

In view of the aforementioned discussion, Kanekawa et al. and Yukutake et al. teachings establishes a prima facie case of obviousness because the teachings and suggestion render the claimed limitations obvious.

And for all the above reasons, the rejection should be sustained.

Respectfully Submitted,

Khanh cong Tran

Khanh Tran

Examiner, Art Unit 2631

October 5, 2005-10-05

Conferee

Mohammed Ghayour

Supervisory Patent Examine, Art Unit 2631

Conferee

Stephen Chin

STEPHEN CHIN
SUPERVISORY PATENT EXAMINE
TECHNOLOGY CENTER 2600

Supervisory Patent Examine, Art Unit 2634